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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,921	08/24/2001	Walter Clark Milliken	BBNT-P01-128	3501

28120 7590 08/11/2006

FISH & NEAVE IP GROUP
ROPES & GRAY LLP
ONE INTERNATIONAL PLACE
BOSTON, MA 02110-2624

EXAMINER	
NGUYEN, QUANG N	
ART UNIT	**PAPER NUMBER**
2141	

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,921	MILLIKEN ET AL.	
	Examiner	Art Unit	
	Quang N. Nguyen	2141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 18-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 18-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. In the view of the Appeal Brief filed on 05/24/2006, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office Action is non-final) or a reply under 37 CFR 1.113 (if this Office Action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidences are permitted. See 37 CFR 1.193(b)(2).

Claims 1-16 and 18-21 are presented for examination.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claim 21 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

4. Claim 21 is directed to non-statutory subject matter because it appears to have no substantial practical application. To satisfy section 35 USC § 101 requirements, the claim must be for a practical application of a 35 USC § 101 judicial exception. A practical application of a 35 USC § 101 judicial exception is claimed if the claimed invention physically transforms an article or physical object to a different state or thing, or if the claimed invention otherwise produces a useful, concrete, and tangible result.

Claim 21 does not appear to result in a physical transformation nor does it appear to produce a useful, concrete, and tangible result. Specially, it does not appear to produce a tangible result because merely describing "a ternary content addressable memory coupled to a register unit and an operations unit within an arithmetic logic unit" fails to describe, to use, or to make available for use, the result of the description in order to enable its functionality and usefulness to be realized. The practical application is not explicitly recited in the claim nor does it flow inherently therefrom, thus, claim 21 appears to be directed to non-statutory subject matter.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-6, 8-15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Curtis et al. (US 6,000,016), hereinafter "Curtis", in view of Nataraj et al. (US 6,757,779), hereinafter "Nataraj".

7. As to claim 1, **Curtis** teaches a central processing unit CPU *(i.e., microprocessor 80 as in Fig. 2)*, comprising:

an arithmetic logic unit *(ALU 0 and ALU 1 as in Fig. 2)*; and

a content addressable memory *(i.e., bypass network 110 includes a content addressable memory array CAM 128)* operatively coupled to the arithmetic logic unit within the CPU *(i.e., within the microprocessor 80)* and configured to perform one or more matching operations *(wherein the CAM includes comparators that compare destination addresses with source addresses)* **(Curtis, Fig. 2, col. 3 lines 15-50 and col. 4, lines 31-48)**.

However, **Curtis** does not explicitly teach the content addressable memory is a ternary content addressable memory (ternary CAM or TCAM).

In an analogous art, **Nataraj** teaches a policy-based router can use a content addressable memory (CAM)-based system to implement a filtering or classification function to determine whether an incoming packet matches a policy statement *(i.e., matching network addresses)*, wherein a ternary CAM array 304/404 is used to store policy statements and mask data to be compared with processed policy information of an incoming packet **(Nataraj, Figs. 3-4, col. 2, lines 12-32 and col. 7, lines 38-65)**.

Therefore, it would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention to incorporate the feature of the content addressable memory (CAM) is a ternary content addressable memory (TCAM), as disclosed by **Nataraj**, into the teaching of **Curtis**, since a ternary CAM requires a smaller number of table entries to represent each hierarchical address than a binary CAM *(a single ternary entry "1XX" can be represented by 4 binary entries "100", "101", "110" and "111")*, therefore, using a ternary CAM in place of a binary CAM would reduce a number of searches of the CAM needed in the worst case to find a matching entry.

8. As to claim 2, **Curtis-Nataraj** teaches the CPU of claim 1, wherein the one or more matching operations include a network packet processing operation *(Curtis teaches the CAM includes comparators that compare the destination address with a source address)* **(Curtis, Abstract, col. 2, lines 39-44, col. 6, lines 1-31 and Nataraj, col. 16, line 47 – col. 17, line 5)**.

9. As to claim 3, **Curtis-Nataraj** teaches the CPU of claim 2, wherein the packet processing operation includes an address lookup operation **(Curtis, Abstract, col. 2, lines 39-44, col. 6, lines 1-31 and Nataraj, col. 16, line 47 – col. 17, line 5)**.

10. As to claim 4, **Curtis-Nataraj** teaches the CPU of claim 3, wherein the address lookup operation includes an Internet Protocol (IP) address lookup operation **(Curtis, Abstract, col. 2, lines 39-44, col. 6, lines 1-31 and Nataraj, col. 16, line 47 – col. 17, line 5)**.

11. As to claim 5, **Curtis-Nataraj** teaches the CPU of claim 1, wherein the one or more matching operations include a packet stuff/unstuffy operation **(Curtis, Abstract, col. 2, lines 39-44, col. 6, lines 1-31 and Nataraj, col. 14, line 27 – col. 15, line 13)**.

12. As to claim 6, **Curtis-Nataraj** teaches the CPU of claim 1, wherein the one or more matching operations include a packet classification operation **(Curtis, Abstract, col. 2, lines 39-44, col. 6, lines 1-31 and Nataraj, col. 9, lines 33-63)**.

13. As to claim 8, **Curtis** teaches the CPU of claim 1, but does not further explicitly teach a first register configured to store a first 32-bit operand; and a second register configured to store a second 32-bit operand.

In an analogous art, **Nataraj** teaches a first register configured to store a first 32-bit operand *(i.e., comparand register C1 storing a first 32-bit comparand)*; and a second register configured to store a second 32 bit operand *(i.e., comparand register C2 storing a second 32-bit comparand, such that comparand register pair C1/C2 is coupled/configured to receive a 64 bit value from the data bus 1604 as in Fig. 21)* **(Nataraj, Fig. 21 and col. 37, line 46 – col. 38, line 24)**.

Therefore, it would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention to incorporate the feature of a first register configured to store a first 32-bit operand and a second register configured to store a second 32-bit operand, as disclosed by **Nataraj**, into the teaching of **Curtis**, because it would allow the system to configure and enable a single CAM array to store and

maintain a different table size in each different mode of operation, hence, the processing overhead in searching/matching for any word in excess of 32-bits to be dramatically improved by the flexibility configuration of the CAM array **(Nataraj, col. 22, lines 8-45)**.

14. As to claim 9, **Curtis** teaches the CPU of claim 8, but does not explicitly teach the ternary content addressable memory performs the one or more matching operations based on at least one of the first or second 32-bit operands.

In an analogous art, **Nataraj** teaches the ternary content addressable memory performs the one or more matching operations based on at least one of the first or second 32-bit operands *(i.e., performing the one or more matching operations based on at least one of C1-C8 comparand registers)* **(Nataraj, Fig, 21 and col. 37, line 46 – col. 38, line 24)**.

Therefore, it would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention to incorporate the feature of the ternary content addressable memory performs the one or more matching operations based on at least one of the first or second 32-bit operands, as disclosed by **Nataraj**, into the teaching of **Curtis**, because it would allow the system to configure and enable a single CAM array to store and maintain a different table size in each different mode of operation, hence, the processing overhead in searching/matching for any word in excess of 32-bits to be dramatically improved by the flexibility configuration of the CAM array **(Nataraj, col. 22, lines 8-45)**.

15. As to claim 10, **Curtis** teaches the CPU of claim 8, but does not explicitly teach the ternary content addressable memory includes a memory array including a group of 64-bit entries and wherein, when performing the one or more matching operations, the ternary content addressable memory compares higher order bits of each entry of the memory array to the first 32-bit operand and compares lower order bits of each entry of the memory array to the second 32-bit operand.

In analogous art, **Nataraj** teaches the ternary content addressable memory includes a memory array including a group of 64-bit entries *(i.e., TCAM array 1501/1601 can be configured for x32, x64, x128, or x256 operation, so 64-bits entries will span 2 row segments, for example, S1/S2, S3/S4, S5/S6 and S7/S8 of row* $1522_{1\text{-}Y}$*)*, and wherein, when performing the one or more matching operations, the ternary content addressable memory compares higher order bits of each entry of the memory array to the first 32-bit operand and compares lower order bits of each entry of the memory array to the second 32-bit operand *(i.e., when the system is configured in x64 mode, the 64-bit comparand word is loaded into all 4 comparand register segment pairs C1/C2, C3/C4, C5/C6, C7/C8 simultaneously for comparison with each of the 8 corresponding segments S1-S8 in each row of the TCAM array 1601 as in Fig. 21)* **(Nataraj, Figs. 15 and 21, col. 36, lines 45-62 and col. 37, line 62 - col. 38, line 24)**.

Therefore, it would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention to incorporate the feature of the ternary content addressable memory includes a memory array including a group of 64-bit entries and wherein, when performing the one or more matching operations, the ternary content addressable memory compares higher order bits of each entry of the memory

array to the first 32-bit operand and compares lower order bits of each entry of the memory array to the second 32-bit operand, as disclosed by **Nataraj**, into the teaching of **Curtis**, because it would allow the system to configure and enable a single CAM array to store and maintain a different table size in each different mode of operation, hence, the processing overhead in searching/matching for any word in excess of 32-bits to be dramatically improved by the flexibility configuration of the CAM array **(Nataraj, col. 22, lines 8-45)**.

16. As to claim 11, **Curtis** teaches the CPU of claim 1, but does not explicitly teach the ternary content addressable memory includes a memory array that includes a group of 64-bits entries.

In an analogous art, **Nataraj** teaches the ternary content addressable memory includes a memory array that includes a group of 64-bits entries *(i.e., TCAM array 1501/1601 can be configured for x32, x64, x128, or x256 operation, so 64-bits entries will span 2 row segments, for example, S1/S2, S3/S4, S5/S6 and S7/S8 of row* $1522_{1\text{-}Y}$*)* **(Nataraj, Figs. 15 and 21, col. 22, lines 8-45 and col. 37, line 62 – col. 38, line 24)**.

Therefore, it would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention to incorporate the feature of the ternary content addressable memory includes a memory array that includes a group of 64-bits entries, as disclosed by **Nataraj**, into the teaching of **Curtis**, because it would allow the system to configure and enable a single CAM array to store and maintain a different table size in each different mode of operation, hence, the processing overhead in

searching/matching for any word in excess of 32-bits to be dramatically improved by the flexibility configuration of the CAM array **(Nataraj, col. 22, lines 8-45)**.

17. As to claim 12, **Curtis** teaches the CPU of claim 11, but does not explicitly teach the memory array comprises 32 entries.

In an analogous art, **Nataraj** teaches the memory array comprises 32 entries *(i.e., TCAM array 1501/1601 can be configured for x32, x64, x128, or x256 operation, so 64-bits entries will span 2 row segments of 32 CAM cells per row, for example, S1/S2, S3/S4, S5/S6 and S7/S8 of row* 1522_{1-Y}*, hence, 32 entries of 64-bits will include 8 rows of the TCAM array 1501/1601)* **(Nataraj, Figs. 15 and 21, col. 22, lines 8-45 and col. 37, line 62 – col. 38, line 24)**.

Therefore, it would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention to incorporate the feature of the ternary content addressable memory includes a memory array that includes 32 entries of 64-bits entries, as disclosed by **Nataraj**, into the teaching of **Curtis**, because it would allow the system to configure and enable a single CAM array to store and maintain a different table size in each different mode of operation, hence, the processing overhead in searching/matching for any word in excess of 32-bits to be dramatically improved by the flexibility configuration of the CAM array **(Nataraj, col. 22, lines 8-45)**.

18. As to claim 13, **Curtis** teaches the CPU of claim 1, but does not explicitly teach the ternary content addressable memory is configured to compare an operand to a group of entries.

In an analogous art, **Nataraj** teaches the ternary content addressable memory is configured to compare an operand to a group of entries *(i.e., the TCAM array 404 is configured to compare an operand 168.69.43.100 to a group of entries 168.0.0.0/8, 168.69.0.0/16, and 168.69.62.0/24 as illustrated in Fig. 11)* **(Nataraj, Fig. 11 and col. 16, line 47 – col. 17, line 5)**.

Therefore, it would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention to incorporate the feature of the ternary content addressable memory is configured to compare an operand to a group of entries, as disclosed by **Nataraj**, into the teaching of **Curtis**, because it would allow the system to configure and enable a single CAM array to store and maintain a different table size in each different mode of operation, hence, the processing overhead in searching/matching for any word in excess of 32-bits to be dramatically improved by the flexibility configuration of the CAM array **(Nataraj, col. 22, lines 8-45)**.

19. As to claim 14, **Curtis** teaches the CPU of claim 13, but does not explicitly teach set a first flag when the operand fails to match an entry in the group of entries, and set a second flag when the operand matches multiple entries of the group of entries.

In an analogous art, **Nataraj** teaches the ternary content addressable memory is configured to set a first flag when the operand fails to match an entry in the group of entries, and set a second flag when the operand matches multiple entries of the group of entries *(i.e., the CAM device 1200 includes a TCAM array 1201, address logic 1209, comparand register 1207, etc., and further includes logic for generating match flag,*

multiple match flag and/or full-flag signals) **(Nataraj, col. 17, lines 15-22 and col. 18, lines 14-28)**.

Therefore, it would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention to incorporate the feature of the ternary content addressable memory is configured to set a first flag when the operand fails to match an entry in the group of entries, and set a second flag when the operand matches multiple entries of the group of entries, as disclosed by **Nataraj**, into the teaching of **Curtis**, because it would allow the system to configure and enable a single CAM array to store and maintain a different table size in each different mode of operation, hence, the processing overhead in searching/matching for any word in excess of 32-bits to be dramatically improved by the flexibility configuration of the CAM array **(Nataraj, col. 22, lines 8-45)**.

20. As to claim 15, **Curtis** teaches the CPU of claim 13, but does not explicitly teach the ternary content addressable memory is configured to sequentially load the group of entries from a succession of mask/value pairs transferred to the ternary content addressable memory.

In an analogous art, Nataraj teaches the ternary content addressable memory is configured to sequentially load the group of entries from a succession of mask/value pairs transferred to the ternary content addressable memory *(i.e., the TCAM array 404 is configured to sequentially load a group of entries such as 168.0.0.0/8, 168.69.0.0/16, and 168.69.62.0/24 into to compare with a comparand/search key 168.69.43.100 as illustrated in Fig. 11)* **(Nataraj, Fig. 11 and col. 16, line 47 – col. 17, line 5)**.

Therefore, it would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention to incorporate the feature of the ternary content addressable memory is configured to sequentially load the group of entries from a succession of mask/value pairs transferred to the ternary content addressable memory, as disclosed by **Nataraj**, into the teaching of **Curtis**, because it would allow the system to configure and enable a single CAM array to store and maintain a different table size in each different mode of operation, hence, the processing overhead in searching/matching for any word in excess of 32-bits to be dramatically improved by the flexibility configuration of the CAM array **(Nataraj, col. 22, lines 8-45)**.

21. Claim 20 recites a system that contains substantially the same limitations as recited in claim 1; therefore, it is rejected under the same rationale.

22. Claims 7, 16 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Curtis, in view of Nataraj, and further in view of Zuraski, Jr. et al. (US 6,560,740), hereinafter "Zuraski".

23. As to claim 7, **Curtis-Nataraj** teaches the CPU of claim 1, but does not explicitly teach the ternary content addressable memory is located within the arithmetic logic unit.

In an analogous art, **Zuraski** teaches a content addressable memory CAM 82 is located within a repair logic unit 70, as illustrated in Fig. 8, to compare provided address signals with the contents of memory locations within the CAM 82 to determine a match **(Zuraski, Fig. 8 and col. 9, lines 47-60)**.

Therefore, it would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention to incorporate the feature of locating the (ternary) content addressable memory within the (arithmetic) logic unit, as disclosed by **Zuraski**, into the teaching of **Curtis-Nataraj**, because embedding/integrating the ternary content addressable memory within the arithmetic logic unit would provide support hardware-based searching/matching engine functions by quickly examining incoming packets (address information/signals) and forwarding them to other systems in the network for further processing.

24. Claim 16 recites a method that contains substantially the same limitations as recited in claim 1 and 7; therefore, it is rejected under the same rationale.

25. Claim 18 recites a method that contains substantially the same limitation as recited in claim 3; therefore, it is rejected under the same rationale.

26. Claim 19 recites a method that contains substantially the same limitation as recited in claim 6; therefore, it is rejected under the same rationale.

27. Claim 21 rejected under 35 U.S.C. 103(a) as being unpatentable over Zuraski, in view of Nataraj.

28. As to claim 21, **Zuraski** teaches an arithmetic logic unit *(i.e., a Built-In-Self-Test BIST logic unit 20 of Fig. 6)*, comprising:

a register unit *(a memory status register 68 of Fig. 6)*;

an operations unit *(a data comparator 66 of Fig. 6)*; and

a content addressable memory *(a repair LU 70 of Fig. 6 having CAM 82 as in Fig. 8)* coupled to the register unit and the operations unit within the arithmetic logic unit.

However, **Zuraski** does not explicitly teach the content addressable memory is a ternary content addressable memory (ternary CAM or TCAM).

In an analogous art, **Nataraj** teaches a policy-based router can use a content addressable memory (CAM)-based system to implement a filtering or classification function to determine whether an incoming packet matches a policy statement *(i.e., matching network addresses)*, wherein a ternary CAM array 304/404 is used to store policy statements and mask data to be compared with processed policy information of an incoming packet **(Nataraj, Figs. 3-4, col. 2, lines 12-32 and col. 7, lines 38-65)**.

Therefore, it would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention to incorporate the feature of the content addressable memory (CAM) is a ternary content addressable memory (TCAM), as disclosed by **Nataraj**, into the teaching of **Zuraski**, since a ternary CAM requires a smaller number of table entries to represent each hierarchical address than a binary CAM *(a single ternary entry "1XX" can be represented by 4 binary entries "100", "101", "110" and "111")*, therefore, using a ternary CAM in place of a binary CAM would reduce a number of searches of the CAM needed in the worst case to find a matching entry.

Conclusion

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Takahashi (US 5,519,649) discloses a microprocessor includes an arithmetic logic unit (ALU) and a content addressable memory for comparison operations.
- Braceras et al. (US 5,638,315) disclose a content addressable memory for a data processing system.
- Chopra et al. (US 6,510,509) disclose a high-speed rule processor using an array of compare engines that operate in parallel.

30. A shortened statutory period for reply to this action is set to expire THREE (3) months from the mailing date of this communication. See 37 CFR 1.134.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang N. Nguyen whose telephone number is (571) 272-3886.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's SPE, Rupal Dharia, can be reached at (571) 272-3880. The fax phone number for the organization is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quang N. Nguyen
Patent Examiner
AU - 2141